

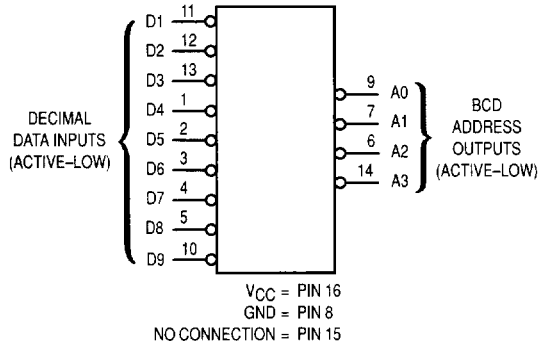
## Decimal-to-BCD Encoder High-Performance Silicon-Gate CMOS

The MC74HC147 is identical in pinout to the LS147. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

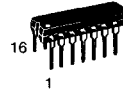
This device encodes nine active-low data inputs to four active-low BCD Address Outputs, ensuring that only the highest order active data line is encoded. The implied decimal zero condition is encoded when all nine data inputs are at a high level (inactive).

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates

**LOGIC DIAGRAM**



## MC74HC147



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08

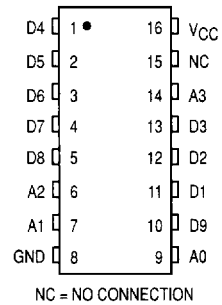


**D SUFFIX**  
SOIC PACKAGE  
CASE 751B-05

**ORDERING INFORMATION**

MC74HCXXXN Plastic  
MC74HCXXXD SOIC

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs								Outputs				
D9	D8	D7	D6	D5	D4	D3	D2	D1	A3	A2	A1	A0
H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	L
H	H	H	H	H	H	H	L	X	H	H	L	H
H	H	H	H	H	H	L	X	X	H	H	L	L
H	H	H	H	H	L	X	X	X	H	L	H	H
H	H	H	H	L	X	X	X	X	H	L	H	L
H	H	H	L	X	X	X	X	X	H	L	L	H
H	H	L	X	X	X	X	X	X	H	L	L	L
H	L	X	X	X	X	X	X	X	L	H	H	H
L	X	X	X	X	X	X	X	X	L	H	H	L



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

**3****DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	V
			6.0	5.48	5.34	5.20	
			2.0	0.1	0.1	0.1	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			6.0	0.1	0.1	0.1	
			2.0	0.1	0.1	0.1	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	V
			6.0	0.26	0.33	0.40	
			2.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2.

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input D to Output A (Figures 1 and 2)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

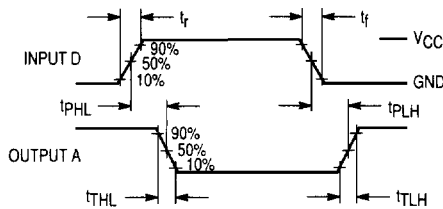
NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2.
2. Information on typical parametric values can be found in Chapter 2.

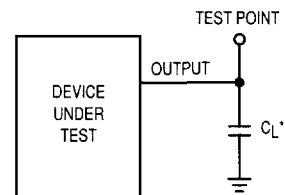
$C_{PD}$	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, VCC = 5.0 V		pF
		35		

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2.

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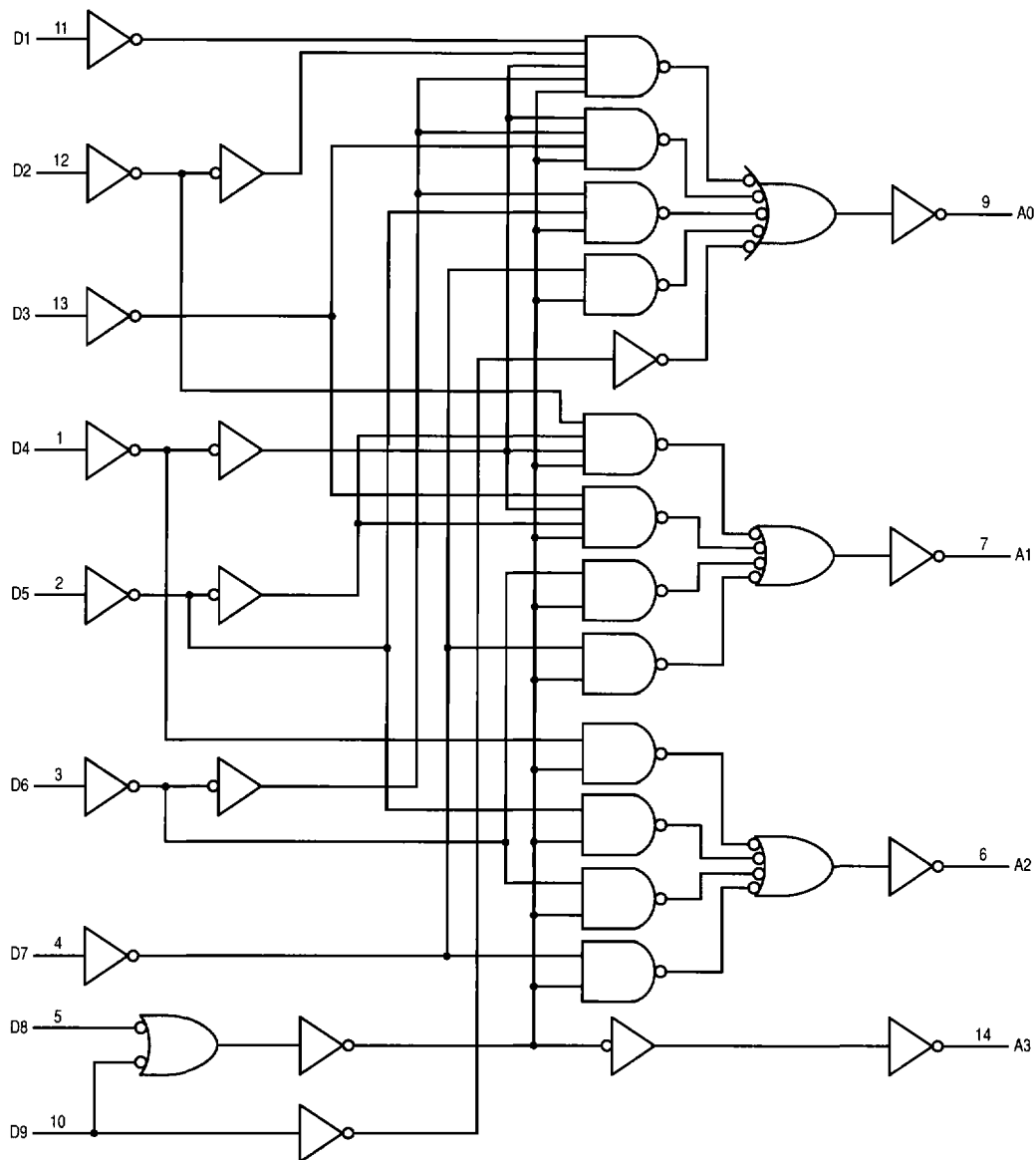
**Figure 1. Switching Waveforms**



\* Includes all probe and jig capacitance

**Figure 2. Test Circuit**

EXPANDED LOGIC DIAGRAM



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