OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS165B – JUNE 1982 – REVISED JULY 1995

- **3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Buffered Control Inputs**
- **SN74ALS575A and ′AS575 Have Synchronous Clear**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N, NT) and Ceramic (J, JT) 300-mil DIPs, and Ceramic Flat (W) Packages**

description

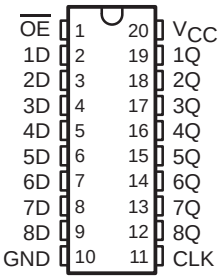
These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN74ALS575A, SN54AS575, and SN74AS575 may be synchronously cleared by taking the clear ($\overline{CLR}$) input low.

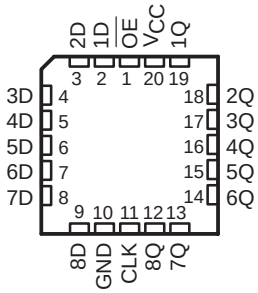
The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS574B, SN54AS574, and SN54AS575 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS574B, SN74ALS575A, SN74AS574, and SN74AS575 are characterized for operation from 0°C to 70°C.

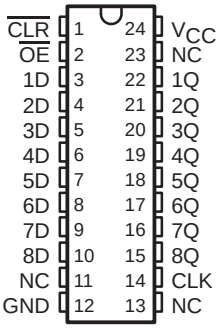
SN54ALS574B, SN54AS574 . . . J OR W PACKAGE
SN74ALS574B, SN74AS574 . . . DW OR N PACKAGE
(TOP VIEW)



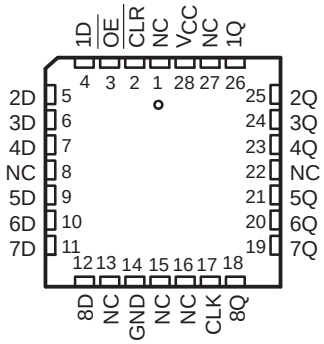
SN54ALS574B, SN54AS574 . . . FK PACKAGE
(TOP VIEW)



SN54AS575 . . . JT OR W PACKAGE
SN74ALS575A, SN74AS575 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS575 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Function Tables

SN54ALS574B, SN74ALS574B, SN54AS574, SN74AS574
(each flip-flop)

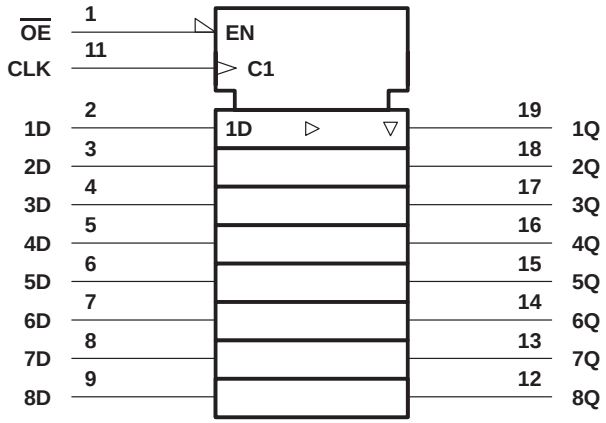
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

SN74ALS575A, SN54AS575, SN74AS575
(each flip-flop)

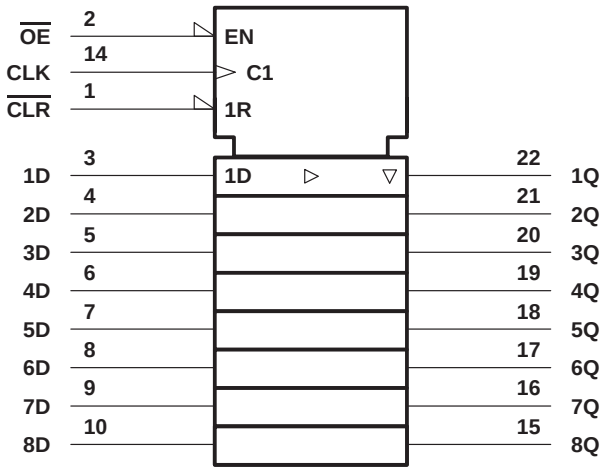
INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	H	X	Z

logic symbols†

SN54ALS574B, SN74ALS574B, SN54AS574, SN74AS574



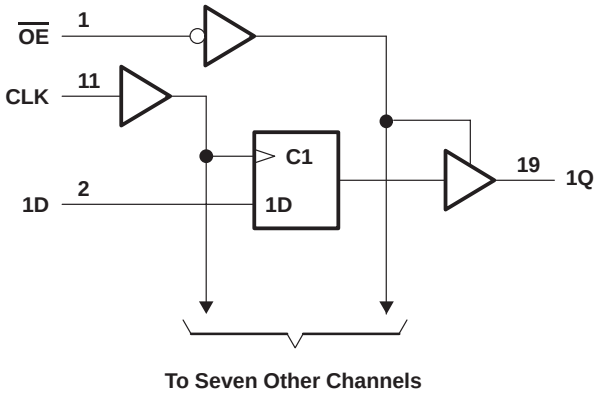
SN74ALS575A, SN54AS575, SN74AS575



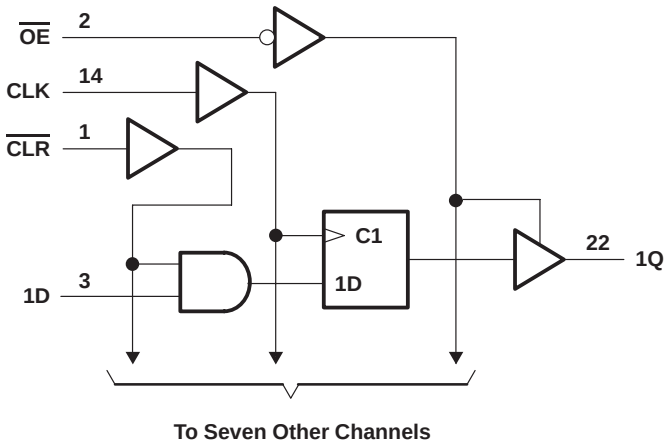
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, JT, N, and NT packages.

logic diagrams (positive logic)

SN54ALS574B, SN74ALS574B, SN54AS574, SN74AS574



SN74ALS575A, SN54AS575, SN74AS575



Pin numbers shown are for the DW, J, JT, N, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS574B . . . . . –55°C to 125°C
SN74ALS574B, SN74ALS575A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS574B			SN74ALS574B SN74ALS575A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				–1			–2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	′ALS574B	0		28	0		35	MHz
		SN74ALS575A				0		30	
t_w	Pulse duration	′ALS574B, CLK high or low	16.5			14			ns
		SN74ALS575A, CLK high or low				16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		SN74ALS575A, $\overline{CLR}$				15			
t_h	Hold time after CLK↑	Data	4			0			ns
		SN74ALS575A, $\overline{CLR}$				0			
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS574B			SN74ALS574B SN74ALS575A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} –2			V_{CC} –2			V
		V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4	3.3					
			I_{OH} = –2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			–20			–20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}	′ALS574B	V_{CC} = 5.5 V	Outputs high		11	18		11	18	mA
			Outputs low		17	27		17	27	
			Outputs disabled		17	28		17	28	
	SN74ALS575A	V_{CC} = 5.5 V	Outputs high		10	17		10	17	
			Outputs low		15	24		15	24	
			Outputs disabled		16	30		16	30	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§						UNIT
			SN54ALS574B		SN74ALS574B		SN74ALS575A		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			28		35		30		MHz
t_{PLH}	CLK	Q	4	22	3	14	4	14	ns
t_{PHL}			4	17	4	14	4	14	
t_{PZH}	$\overline{OE}$	Q	4	21	3	18	4	18	ns
t_{PZL}			4	26	4	18	4	18	
t_{PHZ}	$\overline{OE}$	Q	2	16	1	10	2	10	ns
t_{PLZ}			2	25	2	12	3	13	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54AS574, SN54AS575 . . . . . –55°C to 125°C
SN74AS574, SN74AS575 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				–12			–15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}*	Clock frequency		0		100	0		90	MHz
t_w*	Pulse duration	CLK high	5			5.5			ns
		CLK low	4			5.5			
t_{su}*	Setup time before CLK↑	Data	3			5.5			ns
		′AS575, $\overline{CLR}$ high or low	6.5			6.5			
t_h*	Hold time after CLK↑	Data	3			3			ns
		′AS575, $\overline{CLR}$	0			0			
T_A	Operating free-air temperature		–55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} –2			V_{CC} –2			V
		V_{CC} = 4.5 V	I_{OH} = –12 mA	2.4	3.2					
			I_{OH} = –15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 32 mA		0.29	0.5				V
			I_{OL} = 48 mA					0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			–50			–50	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	$\overline{OE}$, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5			–0.5	mA
	D					–3			–2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}	′AS574	V_{CC} = 5.5 V	Outputs high		73	116		73	116	mA
			Outputs low		85	134		85	134	
			Outputs disabled		84	134		84	134	
	′AS575	V_{CC} = 5.5 V	Outputs high		78	126		78	126	
			Outputs low		89	142		89	142	
			Outputs disabled		88	142		88	142	

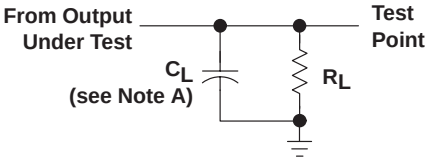
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

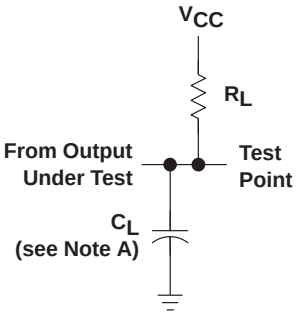
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54AS574 SN54AS575		SN74AS574 SN74AS575		
			MIN	MAX	MIN	MAX	
f_{max}*			100		90		MHz
t_{PLH}	CLK	Any Q	3	11	3	8	ns
t_{PHL}			4	11	4	9	
t_{PZH}	$\overline{OE}$	Any Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OE}$	Any Q	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

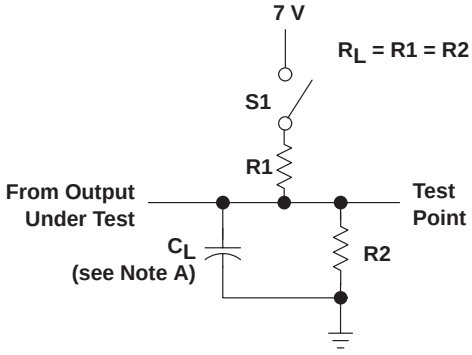
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



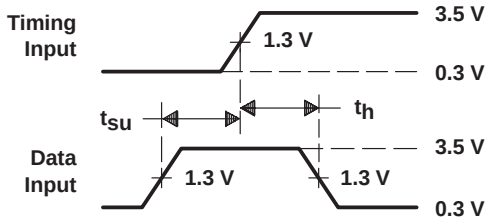
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



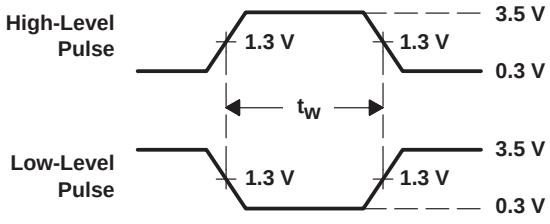
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



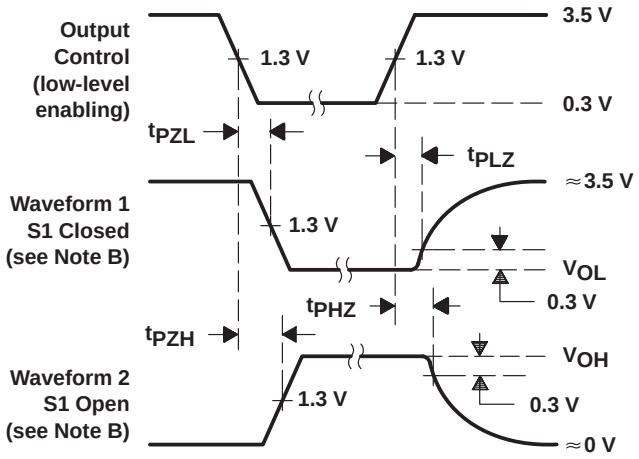
LOAD CIRCUIT FOR 3-STATE OUTPUTS



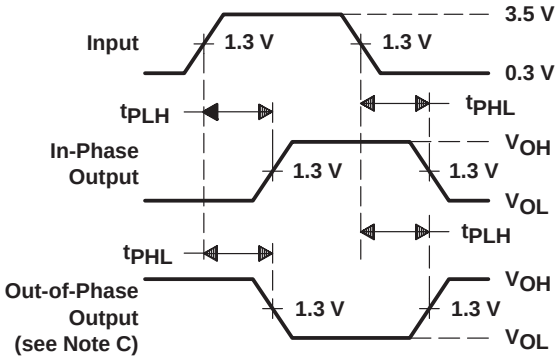
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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SN54AS575, Octal D-type Edge-Triggered Flip-Flops With 3-State Outputs

Device Status: Active

Parameter Name	SN54AS575
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	TTL
No. of Outputs	8
Logic	True

Description

These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN74ALS575A, SN54AS575, and SN74AS575 may be synchronously cleared by taking the clear ($\overline{CLR}$) input low.

The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS574B, SN54AS574, and SN54AS575 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS574B, SN74ALS575A, SN74AS574, and SN74AS575 are characterized for operation from 0°C to 70°C.

Features

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- SN74ALS575A and ´AS575 Have Synchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N, NT) and Ceramic (J, JT) 300-mil DIPs, and Ceramic Flat (W) Packages

To view the following documents, Acrobat Reader 3.x is required.
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Datasheets

Full datasheet in Acrobat PDF: sdas165b.pdf (129 KB)
Full datasheet in Zipped PostScript: sdas165b.psz (129 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (ºC)	Status	Price/unit USD (100-999)	Pack Qty	DSCC Number	Availability / Samples
5962-9754901QKA	W	24	-55 TO 125	ACTIVE	15.45	1		Check stock or order
SN54AS575JT	JT	24	-55 TO 125	ACTIVE	5.93	1		Check stock or order
SNJ54AS575FK	FK	28	-55 TO 125	ACTIVE	15.45	1	5962-9754901Q3A	Check stock or order
SNJ54AS575JT	JT	24	-55 TO 125	ACTIVE	7.43	1	5962-9754901QLA	Check stock or order
SNJ54AS575W	W	24	-55 TO 125	OBSOLETE				

Application Reports

View Application Reports for Digital Logic

- Advanced Schottky (ALS and AS) Logic Families (SDAA010 - Updated: 08/01/1995)
- Advanced Schottky Load Management (SDYA016 - Updated: 02/01/1997)
- Designing With Logic (SDYA009C - Updated: 06/01/1997)
- Input And Output Characteristics Of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

Related Documents

- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB - Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB - Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 284 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (SCAU001A, 850 KB - Updated: 03/01/1996)

Table Data Updated on: 9/7/2000